

What is Claimed:

- 1                   1. A method of fabricating a semiconductor chip including a top  
2 passivation layer formed over the chip comprising the step of:  
3                   forming at least two alignment marks in or on the passivation layer.
- 1                   2. The method according to claim 1 further comprising the step of  
2 selectively processing a portion of the chip using the marks to locate said portion, the  
3 processing selected from etching and adding material.
- 1                   3. The method according to claim 1 wherein the alignment marks  
2 comprise a metal formed on a top surface of the passivation layer.
- 1                   4. The method according to claim 1 wherein the chip includes an  
2 additional underlying passivation layer, and the alignment marks are formed by  
3 depositing material over the underlying passivation layer, and then covering with the top  
4 passivation layer.
- 1                   5. The method according to claim 1 wherein the alignment marks  
2 comprise etched areas formed in the top surface of the top passivation layer.
- 1                   6. The method according to claim 1 wherein the marks are in the shape of  
2 crosses.
- 1                   7. The method according to claim 6 wherein the marks include rectangular  
2 portions at one or more ends of the crosses, the number of portions depending upon the  
3 quadrant of the chip in which the mark is positioned.
- 1                   8. The method according to claim 1 wherein there are at least four  
2 alignment marks, one at each corner of the chip.
- 1                   9. A semiconductor chip comprising:  
2 a passivation layer as a top layer; and  
3 at least two alignment marks formed in or on the passivation layer to  
4 provide topological features for locating selected areas of the chip.
- 1                   10. The chip according to claim 9 wherein the alignment marks comprise a  
2 metal formed on a top surface of the passivation layer.
- 1                   11. The chip according to claim 9 wherein the chip includes an additional  
2 underlying passivation layer, and the alignment marks are formed by material formed  
3 over the underlying passivation layer and covered by the top passivation layer.

1                    12. The chip according to claim 9 wherein the alignment marks comprise  
2 etched areas formed in the top surface of the top passivation layer.

1                    13. The chip according to claim 9 wherein the marks are in the shape of  
2 crosses.

1                    14. The chip according to claim 13 wherein the marks include rectangular  
2 portions at one or more ends of the crosses, the number of portions depending upon the  
3 quadrant of the chip in which the mark is positioned.

1                    15. The chip according to claim 9 wherein there are at least four alignment  
2 marks, one at each corner of the chip.